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WEIDE & MILLER, LTD. 7251 W. LAKE MEAD BLVD. SUITE 530 LAS VEGAS, NV 89128			EXAMINER HU, RUI MENG	
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary

Application No.

10/821,531

Applicant(s)

ALI ET AL.

Examiner

RuiMeng Hu

Art Unit

2618

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 09 April 2004.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-27 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-27 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 09 April 2004 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
 - ☐ Certified copies of the priority documents have been received in Application No. _____.
 - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO/SB/08)
Paper No(s)/Mail Date 08/23/2004.
- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____
- 5) ☐ Notice of Informal Patent Application
- 6) ☐ Other: _____

DETAILED ACTION

Information Disclosure Statement

1. The information disclosure statement submitted on 08/23/2004 been considered by the Examiner and made of record in the application file.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

3. The factual inquiries set forth in *Graham v. John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

4. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to

consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

5. **Claims 1-3, 5-8, 10, 12-14, 16-19, 21-22, 24-25 and 27** are rejected under 35 U.S.C. 103(a) as being unpatentable over **Takenouchi et al. (JP 06-338793)** in view of **Yoshida et al. (US Pub. 2002/0039894)**.

Consider **claim 1**, Takenouchi et al. clearly disclose a method for rapidly generating a signal at an output frequency for use in a communication device comprising (paragraph 1): providing a reference signal (drawing 1, reference signal oscillator 31) at a reference frequency to a first signal synthesizer (drawing 1, PLL 52) configured to generate a first signal at a first frequency; generating the first signal (drawing 1, output of VCO 38) with the first signal synthesizer; processing the first signal to reduce harmonic cross-coupling thereby creating a processed first signal (drawing 1, the first signal is being processed through the first PLL, the circuit of drawing 1 overcomes the problems presented in paragraph 8); providing the reference signal at the reference frequency to a second signal synthesizer (drawing 1, PLL 53) configured to generate a second signal at a second frequency; generating the second signal (drawing 1, output of VCO 39) with the second signal synthesizer; processing the second signal to reduce harmonic cross-coupling (processing the signal through the second PLL) thereby creating a processed second signal; providing the processed first signal and the processed second signal to a switch (drawing 1, switch 42); responsive to a control signal, selectively outputting either the processed first signal or the processed second signal from the switch (paragraph 22).

However Takenouchi et al. fail to disclose responsive to a control signal, selectively dividing, multiplying, or shifting the frequency of the signal output from the switch to thereby generate a frequency specific signal.

In the same field of endeavor, Yoshida et al. clearly disclose responsive to a control signal, selectively dividing, multiplying, or shifting the frequency of the signal output from the synthesizer to thereby generate a frequency specific signal (figure 1, frequency divider 17, paragraphs 70 and 73, the frequency divider 17 is being controllable as to generate a specific frequency for adapt to multiple-mode transmission and reception).

Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate the selection technique taught by Yoshida et al. into the art of Takenouchi et al. as to include controllable frequency modifying means for adapt to multi-mode transmission and reception.

Consider **claim 2 as applied to claim 1**, Takenouchi et al. as modified by Yoshida et al. clearly disclose wherein the first signal synthesizer and the second signal synthesizer comprises phase locked loops or delay locked loops (drawing 1, PLL 32, PLL 33).

Consider **claim 3 as applied to claim 1**, Takenouchi et al. as modified by Yoshida et al. clearly disclose wherein processing the first signal and the second signal to reduce harmonic cross-coupling comprises limit or buffer processing (drawing 1, the first or the second PLL acts as a limiting function, thus a high speed of switching channel is made, as to reduce cross-coupling).

Consider **claim 5 as applied to claim 1**, Takenouchi et al. as modified by Yoshida et al. clearly disclose wherein dividing, multiplying, or shifting comprises modifying the frequency of the signal output from the switch in proportion to the ratio of the output frequency to either the first frequency or the second frequency.

In the same field of endeavor, Yoshida et al. clearly disclose wherein dividing, multiplying, or shifting comprises modifying the frequency of the signal output from the switch in proportion to the ratio of the output frequency to either the first frequency or the second frequency (figure 1, frequency divider 17, paragraphs 70 and 73, the frequency divider 17 is being controllable as to generate a specific frequency to adapt multiple transmission modes).

Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate the selection technique taught by Yoshida et al. into the art of Takenouchi et al. as modified by Yoshida et al. as to include controllable frequency modifying means for adapt to multi-mode transmission and reception.

Consider **claim 6 as applied to claim 1**, Takenouchi et al. as modified by Yoshida et al. clearly disclose further comprising one or more additional signal synthesizers configured to generate one or more additional signals at one or more additional frequencies (paragraph 10, to choose the output of said two or more-circuit PLL frequency synthesizer circuit).

Consider **claim 7 as applied to claim 1**, Takenouchi et al. as modified by Yoshida et al. clearly disclose wherein the first signal synthesizer and the second signal

synthesizer generate signals at frequencies in addition to the first frequency and the second frequency.

In the same field of endeavor, Yoshida et al. clearly disclose an output variable frequency signal of the high frequency synthesizer 11 for adapt to different channels in GSM band (Abstract, paragraph 69).

Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate the selection technique taught by Yoshida et al. into the art of Takenouchi et al. as modified by Yoshida et al. as to generate signals at frequencies in addition to the first and second frequencies as for adapt to different channels.

Consider **claim 8**, Takenouchi et al. clearly disclose a method for generating an output signal at one or more output frequencies comprising (paragraph 22): generating a first signal at a first frequency (figure 1, output of VCO 38); generating a second signal at a second frequency (figure 1, output of VCO 39); providing the first signal and the second signal to a switch (figure 1, SW 42); selectively outputting either of the first signal or the second signal from the switch, and outputting the first signal during a first time period and outputting the second signal during a second time period (paragraphs 25 and 26).

However Takenouchi et al. fail to disclose a frequency modification module; and selectively modifying the frequency of the first signal, the second signal, or both with the frequency modification module.

In the same field of endeavor, Yoshida et al. clearly disclose a frequency modification module; and selectively modifying the frequency of the first signal, the second signal, or both with the frequency modification module (figure 1, frequency divider 17, paragraphs 70 and 73, the frequency divider 17 is being controllable as to generate a specific frequency for adapt to multiple-mode transmission and reception). Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate the selection technique taught by Yoshida et al. into the art of Takenouchi et al. as to include controllable frequency modifying means for adapt to multi-mode transmission and reception.

Consider **claim 10 as applied to claim 8**, Takenouchi et al. as modified by Yoshida et al. clearly disclose further comprising performing a limiting function on at least the first signal or the second signal to reduce cross-coupling (drawing 1, the first or the second PLL acts as a limiting function, thus a high speed of switching channel is made, as to reduce cross-coupling).

Consider **claim 12 as applied to claim 8**, Takenouchi et al. as modified by Yoshida et al. clearly disclose wherein the frequency modification module does not modify the frequency of both the first signal and the second signal (it is optional to include the frequency modification module, the first or second frequency signal could be a specific frequency).

Consider **claim 13 as applied to claim 8**, Takenouchi et al. as modified by Yoshida et al. clearly disclose wherein the frequency modification module modifies the frequency of the first signal by an amount different than the amount of modification to

the frequency of the second signal (In the same of endeavor, Yoshida et al. clearly disclose modifying the frequency signal by different amount as for adapt to different transmission mode (figure 1, frequency divider 17, paragraphs 70 and 73, the frequency divider 17 is being controllable as to generate a specific frequency for adapt to multiple-mode transmission and reception)).

Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate the selection technique taught by Yoshida et al. into the art of Takenouchi et al. as modified by Yoshida et al. as to modify the first and the second signals differently as for adapt to multi-mode transmission and reception.

Consider **claim 14**, Takenouchi et al. clearly disclose a system for generating an output signal, wherein the output signal is capable of being switched between two or more output frequencies (drawing 1), the system comprising: two or more signal generators configured to generate two or more signals (drawing 1, PLL synthesizers 52 and 53), wherein each signal is at a different frequency (paragraph 22); a switch configured to receive at least two signals of the two or more signals and responsive to a control signal output a switch output comprising one of the two or more signals (drawing 1, SW 42 controlled by CPU 43).

However, Takenouchi et al. fail to disclose a frequency modification device configured to receive the switch output and modify the frequency of the switch output to a desired output frequency.

In the same field of endeavor, Yoshida et al. clearly disclose a frequency modification module; and selectively modifying the frequency of the first signal, or the second signal (figure 1, frequency divider 17, paragraphs 70 and 73, the frequency divider 17 is being controllable as to generate a specific frequency for adapt to multiple-mode transmission and reception).

Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate the selection technique taught by Yoshida et al. into the art of Takenouchi et al. as to include controllable frequency modifying means for adapt to multi-mode transmission and reception.

Consider **claim 16 as applied to claim 14**, Takenouchi et al. as modified by Yoshida et al. clearly disclose further comprising a controller configured to generate one or more control signals wherein the control signals synchronize switch output with frequency modification device operation (drawing 1, SW 42 controlled by CPU 43).

In the same field of endeavor, Yoshida et al. clearly disclose (figure 1) a frequency modification device (divider 17) controlled by the controller 19, as for adapt to multi-mode transmission and reception.

Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate the selection technique taught by Yoshida et al. into the art of Takenouchi et al. as modified by Yoshida et al. as to include controllable frequency modifying means for adapt to multi-mode transmission and reception.

Consider **claim 17 as applied to claim 14**, Takenouchi et al. as modified by Yoshida et al. clearly disclose wherein the different frequencies of the two or more signals are selected to minimize cross-coupling between the two or more signals (paragraph 1, a high speed of frequency change reduces cross-coupling).

Consider **claim 18 as applied to claim 14**, Takenouchi et al. as modified by Yoshida et al. clearly disclose wherein the amount of frequency modification performed on a signal is directly proportional to the frequency of a signal and a desired output frequency (In the same field of endeavor, Yoshida et al. clearly disclose wherein the amount of frequency modification performed (figure 1, frequency divider 17) on a signal is directly proportional to the frequency of a signal and a desired output frequency (figure 1, frequency divider 17, paragraphs 70 and 73, consider frequency divider 17 divides the input frequency by 2 as to generate a desired output frequency).

Consider **claim 19 as applied to claim 14**, Takenouchi et al. as modified by Yoshida et al. clearly disclose further comprising a limiter configured to modify the two or more signals prior to switching to reduce cross-coupling between the two or more signals within the switch (drawing 1, the first or the second PLL acts as a limiting function, thus a high speed of switching channel is made, as to reduce cross-coupling).

Consider **claim 21 as applied to claim 14**, Takenouchi et al. as modified by Yoshida et al. clearly disclose wherein the output signal is for use as a local oscillator signal in a wireless communication device (paragraphs 2 and 3).

Consider **claim 22**, Takenouchi et al. clearly disclose a system for rapidly switching the frequency of an output signal between a first frequency and a second

frequency comprising: a switch configured to receive a first signal at a first frequency and a second signal at a second frequency and responsive to a control signal output either of the first signal or the second signal (drawing 1, SW42 controlled by CPU 43 as to output a frequency signal).

However, Takenouchi et al. fail to disclose switching the frequency of an output signal between a third frequency and a fourth frequency, and a frequency modification device configured to, responsive to a control signal, increase or decrease the frequency of a signal output from the switch to either the third frequency or the fourth frequency; and a controller configured to provide to thereby synchronize which signal is output from the switch with frequency modification device operation.

In the same field of endeavor, Yoshida et al. clearly disclose a frequency modification device (figure 1, frequency divider 17) as being controlled by a controller to output different frequency signals by dividing the input frequency signal by 2 or 4 (paragraphs 70 and 73) as for adapt to multi-mode transmission and reception.

Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate the selection technique taught by Yoshida et al. into the art of Takenouchi et al. as to include a controllable frequency modifying means for adapt to multi-mode transmission and reception. Thus Takenouchi et al. as modified by Yoshida et al. clearly disclose switching the frequency of an output signal between a third frequency and a fourth frequency (as switching between different RF bands), and a frequency modification device configured to (Yoshida et al., frequency divider 17 divides the input frequency by 2 or 4), responsive to a control signal,

decrease the frequency of a signal output from the switch to either the third frequency or the fourth frequency; and a controller (Yoshida et al., figure 1, controller 19 controls the divider 17 to generate a frequency signal according to the selected transmission mode) configured to provide to thereby synchronize which signal is output from the switch with frequency modification device operation.

Consider **claim 24 as applied to claim 22**, Takenouchi et al. as modified by Yoshida et al. clearly disclose further comprising one or more limiters configured to modify at least one input to the switch to thereby reduce cross-coupling between the first signal and the second signal (drawing 1, the first or the second PLL acts as a limiting function, thus a high speed of switching channel is made, as to reduce cross-coupling).

Consider **claim 25 as applied to claim 22**, Takenouchi et al. as modified by Yoshida et al. clearly disclose wherein the first frequency and the second frequency are selected to reduce cross-coupling between signals and the system is embodied in an integrated circuit (paragraph 1, a high speed of switching channel reduces cross-coupling, and the multi-circuit PLL frequency synthesizer circuit is an integrated circuit).

Consider **claim 27 as applied to claim 22**, Takenouchi et al. as modified by Yoshida et al. clearly disclose further comprising at least one signal generator (drawing 1, PLL synthesizer 52) configured to generate the first signal, and wherein the controller (drawing 1, paragraph 22, CPU controls the first and the second PLLs 32 and 33 to generate the first and the second frequency signals) is further configured to provide a control signal to at least one signal generator to control which frequency is generated.

Claims 4, 11 and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over **Takenouchi et al. (JP 06-338793)** as modified by **Yoshida et al. (US Pub. 2002/0039894)** in view of **Tahernia et al. (US Patent 4896122)**.

Consider **claim 4 as applied to claim 3**, Takenouchi et al. as modified by Yoshida et al. and Tahernia et al. clearly disclose wherein limit or buffer processing comprises converting a sinusoidal signal to a signal more closely resembling a square wave signal.

In the same field of endeavor, Tahernia et al. clearly disclose wherein processing the oscillating signal comprises buffer processing that comprises converting a sinusoidal signal to a square wave signal (figure 3, column 5 lines 54-66).

Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate the selection technique taught by Tahernia et al. into the art of Takenouchi et al. as modified by Yoshida et al. and Tahernia et al. as to include a buffer for wave-shaping and to provide a square wave oscillating signal as an alternative of the sinusoidal signal.

Consider **claim 11 as applied to claim 10**, Takenouchi et al. as modified by Yoshida et al. fail to disclose wherein the limiting function comprises converting a sinusoidal signal to a signal resembling a square wave signal.

In the same field of endeavor, Tahernia et al. clearly disclose wherein processing the oscillating signal comprises buffer processing that comprises converting a sinusoidal signal to a square wave signal (figure 3, column 5 lines 54-66).

Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate the selection technique taught by Tahernia et al. into the art of Takenouchi et al. as modified by Yoshida et al. as to include a buffer for wave-shaping and to provide a square wave oscillating signal as an alternative of the sinusoidal signal.

Consider **claim 20 as applied to claim 19**, Takenouchi et al. as modified by Yoshida et al. clearly disclose wherein two or more signals generated by the two or more signal generators comprise non-square wave signals (drawing 1, a reference signal oscillator 31).

However, Takenouchi et al. as modified by Yoshida et al. fail to disclose the limiter converts a signal to format more closely approaching a square wave signal.

In the same field of endeavor, Tahernia et al. clearly disclose a limiter converts a signal to format more closely approaching a square wave signal (figure 3, column 5 lines 54-66).

Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate the selection technique taught by Tahernia et al. into the art of Takenouchi et al. as modified by Yoshida et al. as to include a buffer for wave-shaping and to provide a square wave oscillating signal as an alternative of the sinusoidal signal.

Claims 9, 15, 23, 26 are rejected under 35 U.S.C. 103(a) as being unpatentable over **Takenouchi et al. (JP 06-338793)** as modified by **Yoshida et al. (US Pub. 2002/0039894)** in view of **Olip (US Patent 7003274)**.

Consider **claim 9 as applied to claim 8**, Takenouchi et al. as modified by Yoshida et al. fail to disclose wherein the first frequency and the second frequency are non-integer multiples.

In the same field of endeavor, Olip clearly disclose a frequency synthesizer comprises a non-integer frequency multiplier for generating oscillating signals for the first and second RF bands and eliminating spurious mixer products (Abstract).

Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate the selection technique taught by Olip into the art of Takenouchi et al. as modified by Yoshida et al. as to include a non-integer multiplier for improving signal quality.

Consider **claim 15 as applied to claim 14**, Takenouchi et al. as modified by Yoshida et al. fail to disclose wherein the two or more signal generators generate signals that are at frequencies that are non-integer multiples.

In the same field of endeavor, Olip clearly disclose a frequency synthesizer comprises a non-integer frequency multiplier for generating oscillating signals for the first and second RF bands and eliminating spurious mixer products (Abstract).

Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate the selection technique taught by Olip

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into the art of Takenouchi et al. as modified by Yoshida et al. as to include a non-integer multiplier for improving signal quality.

Consider **claim 23 as applied to claim 22**, Takenouchi et al. as modified by Yoshida et al. fail to disclose wherein the frequency modification device comprises a frequency multiplier configured to multiply a received signal by a value necessary to modify the frequency of the received signal to either the third frequency or the fourth frequency.

In the same field of endeavor, Olip clearly disclose a non-integer frequency multiplier for generating oscillating signals for the first and second RF bands and eliminating spurious mixer products (Abstract).

Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate the selection technique taught by Olip into the art of Takenouchi et al. as modified by Yoshida et al. as to include a non-integer multiplier for improving signal quality and an alternate way to achieve the third or the fourth frequency.

Consider **claim 26 as applied to claim 22**, Takenouchi et al. as modified by Yoshida et al. fail to disclose wherein the ratio between the first frequency and the second frequency is a non-integer value.

In the same field of endeavor, Olip clearly disclose a frequency synthesizer comprises a non-integer frequency multiplier for generating oscillating signals for the first and second RF bands and eliminating spurious mixer products (Abstract).

Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate the selection technique taught by Olip into the art of Takenouchi et al. as modified by Yoshida et al. as to include a non-integer multiplier for improving signal quality.

Conclusion

Any response to this Office Action should be **faxed to** (571) 273-8300 **or mailed to:**

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Hand-delivered responses should be brought to

Customer Service Window
Randolph Building
401 Dulany Street
Alexandria, VA 22314

Any inquiry concerning this communication or earlier communications from the examiner should be directed to RuiMeng Hu whose telephone number is 571-270-1105. The examiner can normally be reached on Monday - Thursday, 8:00 a.m. - 5:00 p.m., EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Edan Orgad can be reached on 571-272-7884. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR.

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For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should

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Business Center (EBC) at 866-217-9197 (toll-free).

RuiMeng Hu

R.H./rh

March 13, 2007



3-16-07

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